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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,900	09/20/2005	Shunichi Ishihara	03500.017975.	7137

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EXAMINER	
TAI, XIUYU	
ART UNIT	**PAPER NUMBER**
4151	
MAIL DATE	**DELIVERY MODE**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/549,900	ISHIHARA, SHUNICHI	
	Examiner	Art Unit	
	Xiuyu Tai	4151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/20/2005 & 12/22/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamoto et al (U.S. 5,066,340) in view of Saitoh et al (U.S. 5,677,236) and in view of Itoh et al (Journal of Crystal Growth 45 (1978) 446-453).

4. Regarding claim 1, Iwamoto et al disclose a photovoltaic device. The device comprises: (1) a crystalline layer 1 composed of a polycrystalline silicon semiconductor material (Figure 1; col. 2, line 61; claim 1); (2) a microcrystalline layer 2 is provided on the crystalline layer (Figure 1; col. 2, line 60 61; claim 1); and (3) an n-type amorphous layer 3 is provided on the microcrystalline layer 2 (Figure 1; col. 3, line 1-3; claim 1)

5. Iwamoto fails to teach the layer stacked on polycrystalline silicon having a amorphous silicon phase and a microcrystalline silicon phase. However, Saitoh et al

disclose a thin microcrystalline silicon film in a solar cell. The thin microcrystalline silicon film comprises an amorphous phase with crystallites contained therein (col. 3, line 15-17). Saitoh further teaches that the use of thin microcrystalline silicon film comprising an amorphous phase provides a photovoltaic device having an open-circuit voltage close to that available from one making use of amorphous silicon without substantial reductions in short-circuit current an full factor, having improved light stability and requiring substantially shortened film forming time (col. 6, line 40-45). Therefore, it would be obvious for one having ordinary skill in the art to substitute the microcrystalline silicon layer of Iwanoto with the thin microcrystalline silicon film as taught by Saitoh in order to reduce photo deterioration and to improve light stability in the light of the teaching of Saitoh (col. 4, line 53-54 & col. 6, line 44-45).

6. With respect to silicon substrate as cited in claim 1, the reference of Iwamoto is silent regarding how the crystalline layer 1 is processed. The silicon substrate as cited in claim 1 comprises a high-purity polycrystalline silicon layer. The crystalline layer I of Iwanoto is composed of polycrystalline silicon (col. 2, line 61-62). Therefore, the silicon substrate made with the recited process in claim 1 apparent to be substantially identical with crystalline layer 1 of Iwanoto. Claim 1 is product (polycrystalline silicon ingot) by process (melting metal-grade silicon and solidifying the silicon in one direction) claim. Because of the nature of product-by-process claims, the Examiner cannot ordinarily focus on the precise difference between the claimed product and the disclosed product. It is then Applicants' burden to prove that an unobvious difference exists. See In re Marosi, 218 USPQ 289,292-293 (CAFC 1983). Furthermore, pulling ingot from a melt of

metal grade silicon and growing silicon layers on sliced pulled ingots is a conventional method to make polycrystalline. This method is also taught by Itoh et al (first paragraph in Experimental section). Therefore, it would be obvious for one having ordinary skill in the art to utilize a conventional method of making polycrystalline silicon as taught by Itoh in order to produce polycrystalline silicon with a better established method.

7. Regarding claim 2, Iwamoto further indicates that the microcrystalline layer thickness is preferably not more than 50 nm in order to achieve higher conversion efficiency (col. 3, line 31-36). Therefore, it would be obvious for one having ordinary skill in the art to fabricate the layer having microcrystalline silicon phase and amorphous silicon phase of Iwanoto/Saitoh in the thickness of 1nm to 15 nm in order to achieve higher conversion efficiency in the light of the teaching of Iwanoto ((col. 3, line 31-36).

8. Regarding claim 3, Saitoh teaches that the crystalline fraction should preferably be in a range of from 5 to 80% (col. 4, line 45-47), meaning the ratio of amorphous silicon phase to the microcrystalline silicon phase in a range of from 1:4 (20:80) to19:1(95:5), which is within the range from 1:1 to 10:1as claimed.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamoto et al (U.S. 5,066,340) in view of Saitoh et al (U.S. 5,677,236) and in further view of Yamamoto et al (U.S. 4,959,603).

10. Regarding claim 4, Iwamoto et al disclose a photovoltaic device. The device comprises: (1) a crystalline layer 1 composed of a single crystalline or polycrystalline silicon semiconductor material (Figure 1; col. 2, line 61; claim 1); (2) a microcrystalline layer 2 is provided on the crystalline layer (Figure 1; col. 2, line 60 61; claim 1); and (3)

an n-type amorphous layer 3 is provided on the microcrystalline layer 2 (Figure 1; col. 3, line 1-3; claim 1).

11. Iwamoto fails to teach the layer stacked on polycrystalline silicon having a amorphous silicon phase and a microcrystalline silicon phase. However, Saitoh et al disclose a thin microcrystalline silicon film in a solar cell. The thin microcrystalline silicon film comprises an amorphous phase with crystallites contained therein (col. 3, line 15-17). Saitoh further teaches that the use of thin microcrystalline silicon film comprising an amorphous phase provides a photovoltaic device having an open-circuit voltage close to that available from one making use of amorphous silicon without substantial reductions in short-circuit current an full factor, having improved light stability and requiring substantially shortened film forming time (col. 6, line 40-45). Therefore, it would be obvious for one having ordinary skill in the art to substitute the microcrystalline silicon layer of Iwanoto with the thin microcrystalline silicon film as taught by Saitoh in order to reduce photo deterioration and to improve light stability in the light of the teaching of Saitoh (col. 4, line 53-54 & col. 6, line 44-45).

12. Neither Iwamoto nor Saitoh teaches a polycrystalline silicon layer provided on a layer having amorphous phase and microcrystalline phase. However, Yamamoto et al disclose solar battery equipment. Yamamoto indicates that polycrystalline semiconductor wafer provides a wider range of utility over temperature and higher conversion efficiency compared to amorphous semiconductor material (col.2, line 36-39 & 44-49). Therefore, it would be obvious for one having ordinary skill in the art to substitute the amorphous layer 3 of Iwamoto/Saitoh with a polycrystalline layer as

suggested by Yamamoto in order to improve conversion efficiency of solar cell of Iwanoto/Saitoh.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuyu Tai whose telephone number is 571-270-1855. The examiner can normally be reached on Monday - Friday, 7:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mikhail Kornakov can be reached on 571-272-1303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Xiuyu Tai

3/17/2008

/Michael Kornakov/

Supervisory Patent Examiner, Art Unit 4151